IN THE CLAIMS

1. (Previously Presented) A memory device comprising:

a volatile main memory;

a cache memory connected to the volatile main memory; and

a compression and decompression engine connected between the volatile main memory and the cache memory, wherein the volatile main memory, the cache memory, and the compression and decompression engine are located in a single chip.

2. (Previously Presented) The memory device of claim 1 further comprising, on the single chip, an error detection and correction engine connected to the volatile main memory and the compression and decompression engine.

3. (Cancelled)

4. (Previously Presented) A memory device comprising:

a dynamic memory;

a static memory connected to the dynamic memory;

a compression and decompression engine connected between the dynamic memory and the static memory; and

an error detection and correction engine connected to the dynamic memory and the compression and decompression engine, wherein the dynamic memory, the static memory, the compression and decompression engine, and the error detection and correction engine are located in a single chip.

5. (Previously Presented) The memory device of claim 4 wherein the error detection and correction engine is connected between the dynamic memory and the compression and decompression engine.

6. (Previously Presented) A memory device comprising:

an input/output buffer;

a cache memory connected to the input/output buffer;

a compression and decompression engine connected to the cache memory; and

a volatile main memory connected to the compression and decompression engine, wherein the input/output buffer, the cache memory, the compression and decompression engine, and the volatile main memory and are located in a single chip.

7. (Previously Presented) The memory device of claim 6 wherein the compression and decompression engine is connected between the volatile main memory and the cache memory.

8. (Previously Presented) The memory device of claim 7 further comprising, on the single chip, an error detection and correction engine connected to the volatile main memory and the compression and decompression engine.

9. (Previously Presented) A system comprising:

a processor; and

a memory device connected to the processor, the memory device comprising a volatile main memory and a compression and decompression engine connected to the volatile main memory, wherein the volatile main memory and the compression and decompression engine are located in a single chip.

10. (Previously Presented) The system of claim 9 wherein the memory device further comprises ,on the single chip, an error detection correction engine connected to the compression and decompression engine.

11. (Previously Presented) A system comprising:

a processor; and

a memory device connected to the processor, wherein the memory device comprises a volatile main memory, a compression and decompression engine connected to the volatile main memory , and a cache memory connected to the compression and decompression engine,

wherein the volatile main memory, the compression and decompression engine, and the cache memory and are located in a single chip.

12. (Previously Presented) The system of claim 11 wherein the memory device further comprises, on the single chip, an error detection correction engine connected to the compression and decompression engine.

13. (Original) The system of claim 11 further comprising a graphic control card, wherein the graphic control card connects to the memory device.

14. (Original) The system of claim 11 further comprising a video control card, wherein the video control card connects to the memory device.

15. (Previously Presented) A method of increasing a storage density of a memory device, the method comprising:

providing a volatile main memory;

providing a compression and decompression engine; and

connecting the compression and decompression engine to the volatile main memory, wherein the volatile main memory and the compression and decompression engine are located in a single chip.

16. (Previously Presented) The method of claim 15 further comprising:

providing a cache memory in the single chip; and

connecting the cache memory to the compression and decompression engine.

17. (Previously Presented) The method of claim 15 further comprising:

providing an error detection and correction engine in the single chip; and

connecting the error detection and correction engine to the compression and decompression engine.

18. (Previously Presented) A method of operating a memory device, comprising:

receiving input data at a cache memory;

compressing the input data at a compression and decompression engine to produce compressed data; and

storing the compressed data into a volatile main memory, wherein the cache memory, the compression and decompression engine, and the volatile main memory are located in a single chip.

19. (Previously Presented) The method of claim 18 further comprising:

reading the compressed data from the volatile main memory;

decompressing the compressed data at the compression and decompression engine to produced decompressed data; and

reading the decompressed data to the cache memory.

20. (Previously Presented) A method of operating a memory device, comprising:

receiving data at an input/output buffer;

processing the data at a cache memory to produce processed data;

compressing the processed data at a compression and decompression engine to produce compressed data; and

storing the compressed data into a volatile main memory, wherein the input/output buffer, the cache memory, the compression and decompression engine, and the volatile main memory are located in a single chip.

21. (Previously Presented) The method of claim 20 further comprising:

reading the compressed data from the volatile main memory;

decompressing the compressed data at the compression and decompression engine to produced decompressed data;

reading the decompressed data at the cache memory; and

transferring the data to the input/output buffer.

22. (Previously Presented) A memory device comprising:

an input/output buffer;

a static memory connected to the input/output buffer;

a compression and decompression engine connected to the static memory; and

a dynamic memory connected to the compression and decompression engine, wherein the input/output buffer, the static memory, the compression and decompression engine, and the dynamic memory and are located in a single chip.

23. (Previously Presented) The memory device of claim 22 further comprising, on the single chip, an error detection and correction engine connected to the dynamic memory and the compression and decompression engine.

24. (Previously Presented) A system comprising:

a processor; and

a dynamic random access memory device connected to the processor, the dynamic random access memory device including a plurality of memory blocks and a compression and decompression engine connected to the memory blocks, wherein the memory blocks and the compression and decompression engine are located in a single chip.

25. (Previously Presented) The system of claim 24 wherein the memory device further comprises, on the single chip, an error detection correction engine connected to the compression and decompression engine.

26. (Previously Presented) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a plurality of dynamic memory blocks;

a compression and decompression engine connected to the dynamic memory blocks;

and a static memory block connected to the compression and decompression engine; and

an error detection correction engine connected to the compression and decompression engine, wherein the dynamic memory blocks, the compression and decompression engine, the static memory block, and the error detection correction engine are located in a single chip.

27. (Previously Presented) The system of claim 26 further comprising a graphic control card connected to the memory device.

28. (Previously Presented) The system of claim 27 further comprising a video control card connected to the memory device.

29. (Previously Presented) A method of operating on data comprising:
receiving input data;
compressing the input data to produce compressed data;
storing the compressed data;
reading the compressed data; and
decompressing the compressed data, wherein receiving, compressing, storing, reading, and decompressing are performed on a single chip.

30. (Previously Presented) The method of claim 29 further comprising:
detecting for an error during compressing and decompressing; and
correcting the error during compressing and decompressing.

31. (Previously Presented) A method of operating on data comprising:
receiving input data at a static memory block;
compressing the input data to produce compressed data;
storing the compressed data into a dynamic memory block;
reading the compressed data from the dynamic memory block; and

decompressing the compressed data, wherein receiving, compressing, storing, reading, and decompressing are performed on a single chip.

32. (Previously Presented) The method of claim 31 further comprising:
detecting for an error during compressing and decompressing; and
correcting the error during compressing and decompressing.

33. (New) A memory device comprising:
a dynamic memory;
a plurality of static registers connected to the dynamic memory;
a plurality of register controllers, each of the register controllers being connected to one of the static registers;
a compression and decompression engine connected to the dynamic memory and the plurality of static registers; and
an error detection and correction engine connected to the dynamic memory and the compression and decompression engine, wherein the dynamic memory, the plurality of static registers, the plurality of register controllers, the compression and decompression engine, and the error detection and correction engine are located in a single chip.

34. (New) The memory device of claim 33 further comprising an input/output buffer connected to the plurality of static registers.

35. (New) The memory device of claim 33 wherein the dynamic memory includes a plurality of memory banks.

36. (New) A system comprising:
a processor; and
a memory device connected to the processor, the memory device including:
a dynamic memory;
a plurality of static registers connected to the dynamic memory;

a plurality of register controllers, each of the register controllers being connected to one of the static registers;

a compression and decompression engine connected to the dynamic memory and the plurality of static registers; and

an error detection and correction engine connected to the dynamic memory and the compression and decompression engine, wherein the dynamic memory, the plurality of static registers, the plurality of register controllers, the compression and decompression engine, and the error detection and correction engine are located in a single chip.

37. (New) The system of claim 36 further comprising a graphic control card connected to the memory device.

38. (New) The system of claim 37 further comprising a video control card connected to the memory device.

39. (New) A method comprising:

transferring input data to a plurality of static registers;

independently controlling the transferring of the input data at each of the static registers;

compressing the input data to produce compressed data;

storing the compressed data into a dynamic memory;

reading the compressed data from the dynamic memory; and

decompressing the compressed data, wherein transferring, controlling, compressing, storing, reading, and decompressing are performed on a single chip.

40. (New) The method of claim 39 further comprising:

detecting for an error during the compressing and the decompressing; and

correcting the error during the compressing and the decompressing.